AMENDMENTS TO THE SPECIFICATION

- Please amend the Title, which begins on page 1, line 1, as follows:

METHOD OF MANUFACTURING ESD PROTECTION STRUCTURE

- Please add the Cross-Reference to Related Application(s) section beginning on page 1, line 2, as follows:

CROSS-REFERENCE TO RELATED APPLICATION

This is a divisional of co-pending application serial number 09/733,836, filed December 9, 2000.

- Please delete the paragraph, which begins on page 3, line 27.

~~The present invention further provides a transistor structure for ESD protection in an integrated circuit device. A semiconductor substrate has source and drain diffusion regions and respective source and drain wells under the source and drain diffusion regions. A shallow trench isolation formed over the semiconductor substrate and into the semiconductor substrate separates the source and drain diffusion regions and a portion of the source and drain wells. Source and drain contact structures respectively formed on the shallow trench isolation over the source and drain diffusion regions and extend through the shallow trench isolation to contact the source and drain diffusion regions. This structure has a large parasitic "intrinsic" emitter area and makes the source barrier lowering occur deep in the source well.~~

- Please amend the paragraph, which begins on page 4, line 4, as follows:

The present invention further provides a ~~transistor structure and~~ method of manufacture for an ESD protection structure in an integrated circuit device that has a reduced ESD adjustment cycle time which is flexible in process.

- Please amend the paragraph, which begins on page 4, line 7, as follows:

The present invention further provides a ~~transistor structure and~~ method of manufacture for an ESD protection structure in an integrated circuit device that does not use thin oxide and which is easily turned-on.

- Please amend the paragraph, which begins on page 4, line 10, as follows:

The present invention further provides a ~~transistor structure and~~ method of manufacture for an ESD protection structure in an integrated circuit device that has a low trigger-on voltage for sub-deep-quarter-micron process applications.

- Please amend the Abstract section which begins on page 14, line 1, as follows on the next page: